Interference Search

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L2	0	703/13-15.ccls. and (bidirectional and model and hdl and NMOS).clm.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/07/26 17:42
L3	1	703/13-15.ccls. and (bidirectional and model and wire).clm.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/07/26 17:43
L4	0	703/13-15.ccls. and (NMOS and impedance).clm.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/07/26 17:43
L5	0	703/13-15.ccls. and (NMOS and truth and table).clm.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/07/26 17:44
L6	0	703/13-15.ccls. and (NMOS and (truth adj table)).clm.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/07/26 17:45
L7	1	703/13-15.ccls. and (vHDL and vital).clm.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/07/26 17:46
L8	1	703/13-15.ccls. and (port and control and mechanism).clm.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/07/26 17:46
L9	1	703/13-15.ccls. and (port and delay and annotated).clm.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/07/26 17:46

L10	4	703/13-15.ccls. and (port and enable).clm.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/07/26 17:47
L11	9	(US-4963863-$ or US-5202593-$ or US-5396435-$ or US-6442738-$ or US-6496955-$ or US-6553338-$ or US-6587999-$ or US-6751744-$ or US-6763503-$).did.	USPAT	OR	OFF	2005/07/26 17:55
L12	5	(US-5455521-$ or US-5455928-$ or US-5801549-$ or US-6480817-$ or US-6909307-$).did.	USPAT	OR	OFF	2005/07/26 17:57

Inventor Search.

Day : Tuesday
Date: 7/26/2005

PALM INTRANET

Time: 18:36:09

Inventor Name Search Result

Your Search was:

Last Name = GRUPP
First Name = RICHARD

Application#	Patent#	Status	Date Filed	Title	Inventor Name
10906467	Not Issued	030	02/22/2005	MECHANISM TO PROVIDE TEST ACCESS TO THIRD-PARTY MACRO CIRCUITS EMBEDDED IN AN ASIC (APPLICATION-SPECIFIC INTEGRATED CIRCUIT)	GRUPP, RICHARD J.
10709389	Not Issued	020	04/30/2004	ACCESS METHOD FOR EMBEDDED JTAG TAP CONTROLLER INSTRUCTION REGISTERS	GRUPP, RICHARD J.
10605747	Not Issued	020	10/23/2003	MULTI-VALUED OR SINGLE STRENGTH SIGNAL DETECTION IN A HARDWARE DESCRIPTION LANGUAGE	GRUPP, RICHARD J.
09854038	Not Issued	080	05/11/2001	BIDIRECTIONAL WIRE I/O MODEL AND METHOD FOR DEVICE SIMULATION	GRUPP, RICHARD J.
08232536	5537650	150	12/14/1992	METHOD AND APPARATUS FOR POWER MANAGEMENT IN VIDEO SUBSYSTEMS	GRUPP, RICHARD J.

Inventor Search Completed: No Records to Display.

Search Another: Inventor Last Name: GRUPP First Name: RICHARD Search

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Day : Tuesday
Date: 7/26/2005

PALM INTRANET

Time: 18:36:48

Inventor Name Search Result

Your Search was:

Last Name = TSYRKINA
First Name = YELENA

Application#	Patent#	Status	Date Filed	Title	Inventor Name
09854038	Not Issued	080	05/11/2001	BIDIRECTIONAL WIRE I/O MODEL AND METHOD FOR DEVICE SIMULATION	TSYRKINA, YELENA M.

Inventor Search Completed: No Records to Display.

Search Another: Inventor Last Name: TSYRKINA First Name: YELENA Search

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Back to PALM | ASSIGNMENT | OASIS | Home page

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S224	307	703/15.ccls.	USPAT	OR	OFF	2005/07/26 17:38
S223	167	703/16.ccls.	USPAT	OR	OFF	2005/07/26 17:31
S222	319	S221 and model	USPAT	OR	OFF	2005/07/26 17:24
S221	551	S220 and (bidirectional (bi adj directional))	USPAT	OR	OFF	2005/07/26 17:21
S220	5306	703/1-28.ccls.	USPAT	OR	OFF	2005/07/26 17:20
S218	277	703/21.ccls.	USPAT	OR	OFF	2005/07/26 17:19
S217	233	703/25.ccls.	USPAT	OR	OFF	2005/07/26 17:18
S216	157	703/17.ccls.	USPAT	OR	OFF	2005/07/26 17:14
S213	0	timing with simulat$ with input with port with delay	USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/07/26 13:13
S212	0	annotate with timing with simulat$ with input with port with delay	USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/07/26 13:13
S210	1506	annotate timing with simulat$ with input with port with delay	USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/07/26 13:13
S211	1329	S210	USPAT	OR	OFF	2005/07/26 13:11
S209	8	S208 and (wire and delay)	USPAT	OR	OFF	2005/07/26 13:11
S208	233	703/25.ccls.	USPAT	OR	OFF	2005/07/26 12:56
S175	233	703/25.ccls.	USPAT	OR	OFF	2005/07/26 12:56
S207	80	(bus adj repeater) and (model$5 simulat$6)	USPAT	OR	OFF	2005/07/25 19:10
S113	30	("4161786" | "4604689" | "4768188" | "4837788" | "4974153" | "5036473").PN. OR ("5202593"). URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2005/07/25 19:01

S203	0	S202 near wire near load	USPAT	OR	OFF	2005/07/25 18:59
S202	52	verilog near model	USPAT	OR	OFF	2005/07/25 18:59
S201	1	"09/854038"	US-PGPUB	OR	OFF	2005/07/25 18:34
S200	31	("4161786" | "4604689" | "4768188" | "4837788" | "4974153" | "5036473").PN. OR ("5202593"). URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2005/07/25 15:47
S199	1	"5202593".pn.	US-PGPUB; USPAT; USOCR	OR	OFF	2005/07/25 15:47
S198	43	verilog same media same disk$	USPAT	OR	OFF	2005/07/25 15:47
S197	201	S195 and disks	USPAT	OR	OFF	2005/07/25 15:47
S196	1	S195 and CDROM	USPAT	OR	OFF	2005/07/25 15:47
S195	584	verilog and media	USPAT	OR	OFF	2005/07/25 15:47
S194	185	verilog and vHDL and (timing with delay)	USPAT	OR	OFF	2005/07/25 15:47
S193	160	verilog and HDL and (timing with delay)	USPAT	OR	OFF	2005/07/25 15:47
S192	76	input adj2 port adj delay	USPAT	OR	OFF	2005/07/25 15:47
S191	185	input adj2 port adj2 delay	USPAT	OR	OFF	2005/07/25 15:47
S190	197	input and port adj delay	USPAT	OR	OFF	2005/07/25 15:47
S189	51	timing adj report	USPAT	OR	OFF	2005/07/25 15:47
S188	40	S187 and verilog	USPAT	OR	OFF	2005/07/25 15:47
S187	1504	annotate timing with simulat$ with input with port with delay	USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/07/25 15:47
S186	2	S185 and NMOS	USPAT	OR	OFF	2005/07/25 15:47
S185	75	S184 same (simulat$ or emulat$ or model$ or process$ or execut$)	USPAT	OR	OFF	2005/07/25 15:47
S184	267	timing with delay with port	USPAT	OR	OFF	2005/07/25 15:47

Updated East & Classes/Search

S183	29339	timing with delay	USPAT	OR	OFF	2005/07/25 15:47
S182	3	timing with propogation with delay	USPAT	OR	OFF	2005/07/25 15:47
S181	22	S178 with signal	USPAT	OR	OFF	2005/07/25 15:47
S180	0	S178 with signal with integrity	USPAT	OR	OFF	2005/07/25 15:47
S179	1	S178 with directional	USPAT	OR	OFF	2005/07/25 15:47
S178	389	virtual with port with connection	USPAT	OR	OFF	2005/07/25 15:47
S177	2	NMOS with verilog	USPAT	OR	OFF	2005/07/25 15:47
S176	8	S175 and verilog	USPAT	OR	OFF	2005/07/25 15:47
S174	8	crosspoint with NMOS	USPAT	OR	OFF	2005/07/25 15:47
S173	0	HDL same (channel with bi-directional)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/07/25 15:47
S172	141	HDL same channel	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/07/25 15:47
S171	22	S170 and (detection same change)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/07/25 15:47
S170	526	HDL and Channel and (bus or path) and port	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/07/25 15:47
S169	47	HDL and (Bus adj functional adj Model)	US-PGPUB; USPAT; DERWENT	OR	OFF	2005/07/25 15:47
S168	36	S167 and port and matching	US-PGPUB; USPAT; DERWENT	OR	OFF	2005/07/25 15:47

S167	240	HDL same path	US-PGPUB; USPAT; DERWENT	OR	OFF	2005/07/25 15:47
S166	10527	HDL	US-PGPUB; USPAT; DERWENT	OR	OFF	2005/07/25 15:47
S165	11	S164 and path and (change same detection)	US-PGPUB; USPAT; DERWENT	OR	OFF	2005/07/25 15:47
S164	283	HDL same port	US-PGPUB; USPAT; DERWENT	OR	OFF	2005/07/25 15:47
S163	3	S162 and (change same detection)	US-PGPUB; USPAT; DERWENT	OR	OFF	2005/07/25 15:47
S162	82	S161 and HDL	US-PGPUB; USPAT; DERWENT	OR	OFF	2005/07/25 15:47
S161	7980	port same programming	US-PGPUB; USPAT; DERWENT	OR	OFF	2005/07/25 15:47
S160	1	1996KR-0018252	DERWENT	OR	OFF	2005/07/25 15:47
S159	46	(bi-directional with buffer).ti.	US-PGPUB; USPAT; DERWENT	OR	OFF	2005/07/25 15:47
S158	1	1997GB-0024259	US-PGPUB; USPAT; DERWENT	OR	OFF	2005/07/25 15:47
S157	1	"20040162711"	US-PGPUB; USPAT	OR	OFF	2005/07/25 15:47
S156	0	S155 near wire near load	USPAT	OR	OFF	2005/07/25 15:47
S155	52	verilog near model	USPAT	OR	OFF	2005/07/25 15:47
S154	21	("4488354" | "4683384" | "4744084" | "4791357" | "4821173" | "4942317" | "4978633" | "4980889" | "5105373" | "5166937" | "5300835" | "5317698" | "5406147" | "5426591" | "5426739" | "5428750" | "5452229" | "5479123" | "5481484" | "5535223" | "5572437").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2005/07/25 15:47
S153	3	("6480817").URPN.	USPAT	OR	OFF	2005/07/25 15:47
S152	20	model same (I/o near pad)	USPAT	OR	OFF	2005/07/25 15:47

S151	4	S149 same load	USPAT	OR	OFF	2005/07/25 15:47
S150	0	S149 same verilog	USPAT	OR	OFF	2005/07/25 15:47
S149	69	S148 with model	USPAT	OR	OFF	2005/07/25 15:47
S148	1440	simulat$ with wire	USPAT	OR	OFF	2005/07/25 15:47
S147	3311	simulat$ same wire	USPAT	OR	OFF	2005/07/25 15:47
S146	1	"6584598".pn.	USPAT	OR	OFF	2005/07/25 15:47
S145	1	"6496955".pn.	USPAT	OR	OFF	2005/07/25 15:47
S144	1	"5999734".pn.	USPAT	OR	OFF	2005/07/25 15:47
S143	52	half adj duplex adj modem	USPAT	OR	OFF	2005/07/25 15:47
S142	1	NN9012277	DERWENT; IBM_TDB	OR	OFF	2005/07/25 15:47
S141	11	S140 with path	USPAT	OR	OFF	2005/07/25 15:47
S140	355	(interconnect adj2 model$)	USPAT	OR	OFF	2005/07/25 15:47
S139	4	(interconnect adj2 model$) same load same delay	USPAT	OR	OFF	2005/07/25 15:47
S138	76	verilog and tran	USPAT	OR	OFF	2005/07/25 15:47
S137	1	annotate with path with delay	USPAT	OR	OFF	2005/07/25 15:47
S136	33	wire adj load adj model	USPAT	OR	OFF	2005/07/25 15:47
S135	12	S134 same simulat$	USPAT	OR	OFF	2005/07/25 15:47
S134	148	wire adj model	USPAT	OR	OFF	2005/07/25 15:47
S133	1	((wire or path or line) adj (load or delay) adj (simulate$ or emulate$ or model)) same verilog	USPAT	OR	OFF	2005/07/25 15:47
S132	9	("5610833" | "5629860" | "5694344" | "5706206" | "6175947" | "6189131" | "6243653" | "6291254" | "6381730").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2005/07/25 15:47
S131	0	(US-6763503-$).did.	USPAT	OR	OFF	2005/07/25 15:47

S130	5	(model with wire).ti.	USPAT	OR	OFF	2005/07/25 15:47
S129	0	characterize with wire with delay	USPAT	OR	OFF	2005/07/25 15:47
S128	64	model with wire with delay	USPAT	OR	OFF	2005/07/25 15:47
S127	27	timing with annotation with wire	USPAT	OR	OFF	2005/07/25 15:47
S126	34	S125 with timing	USPAT	OR	OFF	2005/07/25 15:47
S125	3100	wire with model	USPAT	OR	OFF	2005/07/25 15:47
S124	0	wire with timing with I/O with model	USPAT	OR	OFF	2005/07/25 15:47
S123	2	(US-5428750-$ or US-5300835-$).did.	USPAT	OR	OFF	2005/07/25 15:47
S122	21	("4488354" | "4683384" | "4744084" | "4791357" | "4821173" | "4942317" | "4978633" | "4980889" | "5105373" | "5166937" | "5300835" | "5317698" | "5406147" | "5426591" | "5426739" | "5428750" | "5452229" | "5479123" | "5481484" | "5535223" | "5572437").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2005/07/25 15:47
S121	1	("6480817").PN.	USPAT	OR	OFF	2005/07/25 15:47
S120	109	S117 same (port or node) same (path or loop or mesh)	USPAT	OR	OFF	2005/07/25 15:47
S119	5	S117 same (Verilog and VHDL)	USPAT	OR	OFF	2005/07/25 15:47
S118	109	S117 same (port or node) same (path or loop or mesh)	USPAT	OR	OFF	2005/07/25 15:47
S117	15280	S115 with S116	USPAT	OR	OFF	2005/07/25 15:47
S116	2356320	(bidirection$ or ((two adj2 way) or inout or duplex)) near$3 (wire or line)	USPAT	OR	OFF	2005/07/25 15:47
S115	184343	(simulat$ or emulat$)	USPAT	OR	OFF	2005/07/25 15:47
S114	79	(bus adj repeater) and (model$5 simulat$6)	USPAT	OR	OFF	2005/05/03 13:58
S111	38	verilog same media same disk$	USPAT	OR	OFF	2005/05/03 13:57
S90	3	timing with propogation with delay	USPAT	OR	OFF	2005/05/03 13:56

S112	1	"5202593".pn.	US-PGPUB; USPAT; USOCR	OR	OFF	2005/05/03 11:21
S110	179	S108 and disks	USPAT	OR	OFF	2004/12/30 16:14
S109	1	S108 and CDROM	USPAT	OR	OFF	2004/12/30 16:14
S108	501	verilog and media	USPAT	OR	OFF	2004/12/30 16:12
S107	169	verilog and vHDL and (timing with delay)	USPAT	OR	OFF	2004/12/29 14:49
S106	145	verilog and HDL and (timing with delay)	USPAT	OR	OFF	2004/12/29 14:49
S96	1402	annotate timing with simulat$ with input with port with delay	USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/12/29 14:32
S104	76	input adj2 port adj delay	USPAT	OR	OFF	2004/12/29 14:31
S103	180	input adj2 port adj2 delay	USPAT	OR	OFF	2004/12/29 14:29
S102	195	input and port adj delay	USPAT	OR	OFF	2004/12/29 14:26
S101	49	timing adj report	USPAT	OR	OFF	2004/12/29 14:25
S100	37	S96 and verilog	USPAT	OR	OFF	2004/12/29 14:01
S94	2	S93 and NMOS	USPAT	OR	OFF	2004/12/29 13:53
S93	71	S92 same (simulat$ or emulat$ or model$ or process$ or execut$)	USPAT	OR	OFF	2004/12/29 13:53
S92	258	timing with delay with port	USPAT	OR	OFF	2004/12/29 13:48
S91	28458	timing with delay	USPAT	OR	OFF	2004/12/29 13:46
S87	1	S86 with directional	USPAT	OR	OFF	2004/12/29 13:42
S89	21	S86 with signal	USPAT	OR	OFF	2004/12/29 10:10
S88	0	S86 with signal with integrity	USPAT	OR	OFF	2004/12/29 10:09
S86	362	virtual with port with connection	USPAT	OR	OFF	2004/12/29 10:06
S85	2	NMOS with verilog	USPAT	OR	OFF	2004/12/29 10:06
S78	8	crosspoint with NMOS	USPAT	OR	OFF	2004/12/28 16:03
S83	7	S81 and verilog	USPAT	OR	OFF	2004/12/28 15:48
S81	227	703/25.ccls.	USPAT	OR	OFF	2004/12/28 15:48

S77	0	HDL same (channel with bi-directional)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/12/27 16:04
S76	121	HDL same channel	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/12/27 15:43
S75	21	S74 and (detection same change)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/12/27 15:41
S74	446	HDL and Channel and (bus or path) and port	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/12/27 15:38
S63	45	(bi-directional with buffer).ti.	US-PGPUB; USPAT; DERWENT	OR	OFF	2004/12/27 15:36
S73	43	HDL and (Bus adj functional adj Model)	US-PGPUB; USPAT; DERWENT	OR	OFF	2004/12/27 15:27
S72	34	S71 and port and matching	US-PGPUB; USPAT; DERWENT	OR	OFF	2004/12/27 15:27
S71	216	HDL same path	US-PGPUB; USPAT; DERWENT	OR	OFF	2004/12/27 15:26
S70	9226	HDL	US-PGPUB; USPAT; DERWENT	OR	OFF	2004/12/27 15:25
S69	8	S68 and path and (change same detection)	US-PGPUB; USPAT; DERWENT	OR	OFF	2004/12/27 15:25
S68	248	HDL same port	US-PGPUB; USPAT; DERWENT	OR	OFF	2004/12/27 15:22
S67	2	S66 and (change same detection)	US-PGPUB; USPAT; DERWENT	OR	OFF	2004/12/27 15:22
S66	72	S65 and HDL	US-PGPUB; USPAT; DERWENT	OR	OFF	2004/12/27 15:20

S65	7229	port same programming	US-PGPUB; USPAT; DERWENT	OR	OFF	2004/12/27 15:20
S64	1	1996KR-0018252	DERWENT	OR	OFF	2004/12/27 14:39
S61	1	1997GB-0024259	US-PGPUB; USPAT; DERWENT	OR	OFF	2004/12/27 14:37
S60	1	"20040162711"	US-PGPUB; USPAT	OR	OFF	2004/12/27 14:05
S54	0	S53 near wire near load	USPAT	OR	OFF	2004/12/27 11:15
S53	49	verilog near model	USPAT	OR	OFF	2004/12/27 11:14
S50	20	model same (I/o near pad)	USPAT	OR	OFF	2004/12/27 11:13
S52	21	("4488354" | "4683384" | "4744084" | "4791357" | "4821173" | "4942317" | "4978633" | "4980889" | "5105373" | "5166937" | "5300835" | "5317698" | "5406147" | "5426591" | "5426739" | "5428750" | "5452229" | "5479123" | "5481484" | "5535223" | "5572437").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2004/12/27 11:07
S51	2	("6480817").URPN.	USPAT	OR	OFF	2004/12/27 11:07
S47	66	S46 with model	USPAT	OR	OFF	2004/12/27 11:02
S49	4	S47 same load	USPAT	OR	OFF	2004/12/27 10:59
S48	0	S47 same verilog	USPAT	OR	OFF	2004/12/27 10:59
S46	1377	simulat$ with wire	USPAT	OR	OFF	2004/12/27 10:58
S45	3184	simulat$ same wire	USPAT	OR	OFF	2004/12/27 10:58
S44	1	"6584598".pn.	USPAT	OR	OFF	2004/12/27 10:58
S43	1	"6496955".pn.	USPAT	OR	OFF	2004/12/27 10:57
S42	1	"5999734".pn.	USPAT	OR	OFF	2004/12/27 10:56
S41	52	half adj duplex adj modem	USPAT	OR	OFF	2004/12/27 10:55
S30	1	NN9012277	DERWENT; IBM_TDB	OR	OFF	2004/12/27 10:32
S29	10	S28 with path	USPAT	OR	OFF	2004/12/23 16:43
S28	315	(interconnect adj2 model$)	USPAT	OR	OFF	2004/12/23 16:42
S27	4	(interconnect adj2 model$) same load same delay	USPAT	OR	OFF	2004/12/23 16:42
S26	66	verilog and tran	USPAT	OR	OFF	2004/12/23 13:53
S19	9	("5610833" | "5629860" | "5694344" | "5706206" | "6175947" | "6189131" | "6243653" | "6291254" | "6381730").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2004/12/23 13:50
S24	1	annotate with path with delay	USPAT	OR	OFF	2004/12/23 13:46
S23	32	wire adj load adj model	USPAT	OR	OFF	2004/12/23 13:46

S22	11	S21 same simulat$	USPAT	OR	OFF	2004/12/23 13:43
S21	129	wire adj model	USPAT	OR	OFF	2004/12/23 13:42
S20	1	((wire or path or line) adj (load or delay) adj (simulate$ or emulate$ or model)) same verilog	USPAT	OR	OFF	2004/12/23 13:42
S15	57	model with wire with delay	USPAT	OR	OFF	2004/12/23 13:37
S18	1	(US-6763503-$).did.	USPAT	OR	OFF	2004/12/23 11:30
S17	4	(model with wire).ti.	USPAT	OR	OFF	2004/12/23 11:28
S16	0	characterize with wire with delay	USPAT	OR	OFF	2004/12/23 11:25
S14	27	timing with annotation with wire	USPAT	OR	OFF	2004/12/23 10:38
S1	177034	(simulat$ or emulat$)	USPAT	OR	OFF	2004/12/23 10:26
S12	32	S11 with timing	USPAT	OR	OFF	2004/12/22 17:02
S11	2968	wire with model	USPAT	OR	OFF	2004/12/22 17:00
S10	0	wire with timing with I/O with model	USPAT	OR	OFF	2004/12/22 17:00
S4	107	S3 same (port or node) same (path or loop or mesh)	USPAT	OR	OFF	2004/12/22 16:59
S9	2	(US-5428750-$ or US-5300835-$).did.	USPAT	OR	OFF	2004/12/22 16:58
S8	21	("4488354" | "4683384" | "4744084" | "4791357" | "4821173" | "4942317" | "4978633" | "4980889" | "5105373" | "5166937" | "5300835" | "5317698" | "5406147" | "5426591" | "5426739" | "5428750" | "5452229" | "5479123" | "5481484" | "5535223" | "5572437").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2004/12/22 16:51
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S6	5	S3 same (Verilog and VHDL)	USPAT	OR	OFF	2004/12/22 16:04
S5	5	S4 same (control$ or detect$ or compar$) same (change or value)	USPAT	OR	OFF	2004/12/22 15:57
S3	14702	S1 with S2	USPAT	OR	OFF	2004/12/22 15:55
S2	2293911	(bidirection$ or ((two adj2 way) or inout or duplex)) near$3 (wire or line)	USPAT	OR	OFF	2004/12/22 15:54

Terms used **bidirectional load model** Found **34,481** of **158,639**

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1 Space-time characteristics of ALOHA protocols in high-speed bidirectional bus networks
Whay Chiou Lee, Pierre A. Humblet
October 1995 **IEEE/ACM Transactions on Networking (TON)**, Volume 3 Issue 5
Full text available: pdf(914.40 KB) Additional Information: full citation, references, index terms

2 Aquarius: Logic simulation on an Engineering Workstation
Andrew Sangster, Jhon Monahan
June 1983 **Proceedings of the 20th conference on Design automation**
Full text available: pdf(606.71 KB) Additional Information: full citation, abstract, references, citings, index terms

Aquarius is an interactive hierarchical logic simulator designed to run in a multiple window (concurrent processing) environment on an Engineering Workstation. This approach lets an engineer iterate conveniently between simulation and modification of the logic model or input patterns. Because Aquarius is hierarchical, any subtree of the model may be simulated, facilitating bottom-up design verification. Aquarius uses an event-driven selective trace algorithm and 9 logic states. I ...

Keywords: Computer-aided engineering, Engineering workstation, Interactive simulation, Logic simulation, MOS simulation

3 An adversarial model for distributed dynamic load balancing
S. Muthukrishnan, Rajmohan Rajaraman
June 1998 **Proceedings of the tenth annual ACM symposium on Parallel algorithms and architectures**
Full text available: pdf(981.89 KB) Additional Information: full citation, references, citings, index terms

4 Fixed-alternate routing and wavelength conversion in wavelength-routed optical networks
Ramu Ramamurthy, Biswanath Mukherjee
June 2002 **IEEE/ACM Transactions on Networking (TON)**, Volume 10 Issue 3

Full text available: pdf(461.95 KB) Additional Information: full citation, abstract, references, index terms

Consider an optical network which employs wavelength-routing crossconnects that enable the establishment of wavelength-division-multiplexed (WDM) connections between node pairs. In such a network, when there is no wavelength conversion, a connection is constrained to be on the same wavelength channel along its route. Alternate routing can improve the blocking performance of such a network by providing multiple possible paths between node pairs. Wavelength conversion can also improve the blocking ...

Keywords: WDM, adaptive routing, alternate routing, lightpath, optical network, wavelength conversion, wavelength routing

5 A performance model of deflection routing in multibuffer networks with nonuniform traffic
Joseph Bannister, Flaminio Borgonovo, Luigi Fratta, Mario Gerla
October 1995 **IEEE/ACM Transactions on Networking (TON)**, Volume 3 Issue 5
Full text available: pdf(1.29 MB) Additional Information: full citation, references, index terms

6 An MOS digital network model on a modified thevenin equivalent for logic simulation
Tsuyoshi Takahashi, Satoshi Kojima, Osamu Yamashiro, Kazuhiko Eguchi, Hideki Fukuda
June 1984 **Proceedings of the 21st conference on Design automation**
Full text available: pdf(387.72 KB) Additional Information: full citation, abstract, references, index terms

A novel analytical model of MOS digital networks, which is based on a modified Thevenin equivalent, is described. The model can handle all the primary circuits inherent in MOS technology, such as transistor logics, wired-ORs, tri-state circuits, charge-share operation, and bidirectional pass transistors etc., with precise estimation of delay time. The model has been implemented in a logic/fault simulator, named HASL-GT. Performance of 4 to 10 k events/sec has been obtained on HIT ...

7 Conservative simulation of load-balanced routing in a large ATM network model
C. D. Pham, H. Brunst, S. Fdida
July 1998 **ACM SIGSIM Simulation Digest , Proceedings of the twelfth workshop on Parallel and distributed simulation**, Volume 28 Issue 1
Full text available: pdf(938.77 KB) Publisher Site Additional Information: full citation, references, citings, index terms

8 DAB: interactive haptic painting with 3D virtual brushes
Bill Baxter, Vincent Scheib, Ming C. Lin, Dinesh Manocha
August 2001 **Proceedings of the 28th annual conference on Computer graphics and interactive techniques**
Full text available: pdf(10.82 MB) Additional Information: full citation, abstract, references, citings, index terms

We present a novel painting system with an intuitive haptic interface, which serves as an expressive vehicle for interactively creating painterly works. We introduce a deformable, 3D brush model, which gives the user natural control of complex brush strokes. The force feedback enhances the sense of realism and provides tactile cues that enable the user to better manipulate the paint brush. We have also developed a bidirectional, two-layer paint model that, combined with a palette interface ...

Keywords: *Human Computer Interaction, deformable brush model, haptics, painting systems*

9 AutoMod II (tutorial session)
Van B. Norman
December 1990 **Proceedings of the 22nd conference on Winter simulation**
Full text available: pdf(587.66 KB) Additional information: full citation, references, citings, index terms

10 Interactive immersion in 3D graphics: Physically based virtual painting
Ming Lin, William Baxter, Vincent Scheib, Jeremy Wendt
August 2004 **Communications of the ACM**, Volume 47 Issue 8
Full text available: pdf(280.71 KB) html(28.71 KB) Additional information: full citation, abstract, references, index terms

Tapping the compelling illusion of physical interaction with paints, brushes, surfaces, color, and light, users express the nuances of their visual and emotional imaginations.

11 An adaptive, non-uniform cache structure for wire-delay dominated on-chip caches
Changkyu Kim, Doug Burger, Stephen W. Keckler
October 2002 **Proceedings of the 10th international conference on Architectural support for programming languages and operating systems**, Volume 37 , 30 , 36 Issue 10 , 5 , 5
Full text available: pdf(1.33 MB) Additional information: full citation, abstract, references, citings

Growing wire delays will force substantive changes in the designs of large caches. Traditional cache architectures assume that each level in the cache hierarchy has a single, uniform access time. Increases in on-chip communication delays will make the hit time of large on-chip caches a function of a line's physical location within the cache. Consequently, cache access times will become a continuum of latencies rather than a single discrete latency. This non-uniformity can be exploited to provide ...

12 The second generation motis mixed-mode simulator
C. F. Chen, C-Y Lo, H. N. Nham, Prasad Subramanlam
June 1984 **Proceedings of the 21st conference on Design automation**
Full text available: pdf(681.47 KB) Additional information: full citation, abstract, references, citings, index terms

This paper describes the second generation MOTIS mixed-mode simulator. In particular, it extends the current modeling capabilities to include resistors, floating capacitors, and bidirectional transmission gates. It employs a relaxation algorithm with local time-step control for timing simulation, and a switch level approach for unit delay simulation. It provides logic and timing verification for general MOS circuits in a mixed-mode environment. The new simulator is being used for pro ...

13 On the stability of shuffle-exchange and bidirectional shuffle-exchange deflection networks
Soung C. Liew
February 1997 **IEEE/ACM Transactions on Networking (TON)**, Volume 5 Issue 1
Full text available: pdf(289.70 KB) Additional information: full citation, references, index terms

Keywords: deflection routing, hot-potato routing, network congestion, network stability,

packet switching, shuffle-exchange network

14 Peer to peer networks: Query-flood DoS attacks in gnutella
Neil Daswani, Hector Garcia-Molina
November 2002 **Proceedings of the 9th ACM conference on Computer and communications security**
Full text available: pdf(465.15 KB) Additional information: full citation, abstract, references, citings, index terms

We describe a simple but effective traffic model that can be used to understand the effects of denial-of-service (DoS) attacks based on query floods in Gnutella networks. We run simulations based on the model to analyze how different choices of network topology and application level load balancing policies can minimize the effect of these types of DoS attacks. In addition, we also study how damage caused by query floods is distributed throughout the network, and how application-level policies ca ...

Keywords: denial-of-service, peer-to-peer, security

15 The *nesC* language: A holistic approach to networked embedded systems
David Gay, Philip Levis, Robert von Behren, Matt Welsh, Eric Brewer, David Culler
May 2003 **ACM SIGPLAN Notices , Proceedings of the ACM SIGPLAN 2003 conference on Programming language design and implementation**, Volume 38 Issue 5
Full text available: pdf(177.98 KB) Additional information: full citation, abstract, references, citings, index terms

We present *nesC*, a programming language for networked embedded systems that represent a new design space for application developers. An example of a networked embedded system is a sensor network, which consists of (potentially) thousands of tiny, low-power "motes," each of which execute concurrent, reactive programs that must operate with severe memory and power constraints.nesC's contribution is to support the special needs of this domain by exposing a programming model that incorporates ...

Keywords: C, TinyOS, components, concurrency, data races, first-order, modules, nesC, programming languages

16 Load balancing, selection sorting on the hypercube
C. G. Plaxton
March 1989 **Proceedings of the first annual ACM symposium on Parallel algorithms and architectures**
Full text available: pdf(1.16 MB) Additional information: full citation, citings, index terms

17 Data file management in shift-register memories
Werner E. Kluge
June 1978 **ACM Transactions on Database Systems (TODS)**, Volume 3 Issue 2
Full text available: pdf(1.22 MB) Additional information: full citation, abstract, references, index terms

The paper proposes a shift-register memory, structured as a two-dimensional array of uniform shift-register loops which are linked by flow-steering switches, whose switch control scheme is tailored to perform with great efficiency data management operations on sequentially organized files. The memory operates in a linear input/output mode to perform record insertion, deletion, and relocation on an existing file, and in a sublinear mode for rapid internal file movement to expedite file posit ...

Keywords: LIFO/FIFO operation modes, data transformations, deletion, insertion, management of sequentially organized files, record retrieval, relocation, shift-register memories, updating

18 Modeling AGV systems using network constructs
Michael W. Sale, Catherine W. Stein
December 1987 **Proceedings of the 19th conference on Winter simulation**

Full text available: pdf(556.22 KB) Additional Information: full citation, abstract, references, citings, index terms

The network world view of SLAM II® has been demonstrated as an effective method for modeling manufacturing processes. An automatic guided vehicle system (AGVS), however, may be difficult because of the special nature of its resources and their activities. This paper presents the Material Handling Extension for SLAM II© (MHEX). The MHEX overcomes these difficulties through a specialized set of network capabilities. This paper begins by describing the unique requirements i ...

19 Earthmover-simulation tool for earthwork planning
Julio C. Martínez
December 1998 **Proceedings of the 30th conference on Winter simulation**

Full text available: pdf(183.00 KB) Additional Information: full citation, references, citings, index terms

20 Adding a vector unit to a superscalar processor
Francisca Quintana, Jesus Corbal, Roger Espasa, Mateo Valero
May 1999 **Proceedings of the 13th international conference on Supercomputing**

Full text available: pdf(1.75 MB) Additional Information: full citation, references, citings, index terms

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Transmission gate modeling in an existing three-value simulator

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Proceedings of the 19th conference on Design automation table of contents
Pages: 676 - 681
Year of Publication: 1982
ISBN 0-89791-020-6
Author Robert M. McDermott
Sponsors SIGDA: ACM Special Interest Group on Design Automation
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ACM: Association for Computing Machinery
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↑ ABSTRACT

Existing three value (0, 1, X,) logic simulators cannot support the use of MOS transmission gates, but this deficiency can be easily eliminated by the addition of one logic value - the high impedance (Z) state. This paper demonstrates that complete transmission gate modeling, including bi-directional operation and Ratio Logic, can be accomplished with this single Z state and explicit node models; and, since four states require the same internal storage as three states, such an enhancement would not require a major software rewrite.

↑ REFERENCES

Note: OCR errors may be found in this Reference List extracted from the full text article. ACM has opted to expose the complete List rather than only correct and linked references.

1 P.L. Flake, P. R. Moorby, G. Musgrave, "Logic Simulation of Bi-Directional Tri-State Gates", Proceedings of the International Conference on Circuits and Computers, Port Chester, New York, October 1-3 1980, pp. 594-600.

2 Will Sherwood, A MOS modelling technique for 4-state true-value hierarchical logic simulation or Karnough knowledge, Proceedings of the eighteenth design automation conference on Design automation, p.775-785, June 29-July 01, 1981, Nashville, Tennessee, United States

3 J. Wantanabe, J. Miura, T. Kurachi, I. Suetsugu, "Seven Value Logic Simulation for MOS LSI Circuits", Proceedings of the International Conference on Circuits and Computers, Port Chester, New York, October 1-3, 1980, pp. 941-944.

↑ CITINGS

P. L. Flake, P. R. Moorby, G. Musgrave, An algebra for logic strength simulation, Proceedings of the twentieth design automation conference on Design automation, p.615-618, June 27-29, 1983, Miami Beach, Florida, United States

↑ INDEX TERMS

Primary Classification:
B. Hardware
↳ **B.6** LOGIC DESIGN

General Terms:
Design

↑ Peer to Peer - Readers of this Article have also read:

- Data structures for quadtree approximation and compression
Communications of the ACM 28, 9
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Ellen Francik , Susan Ehrlich Rudman , Donna Cooper , Stephen Levine
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Proceedings of the 27th ACM/IEEE conference on Design automation
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A MOS modelling technique for 4-state true-value hierarchical logic simulation or Karnough knowledge

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Sponsors: IEEE-CS\DATC : IEEE Computer Society
SIGDA: ACM Special Interest Group on Design Automation
Publisher: IEEE Press Piscataway, NJ, USA

↑ ABSTRACT

Modelling strategies and techniques are given for static and dynamic MOS transistors in a 4-state (0/low, 1/high, Z/high-impedance, U/undefined) logic simulator environment. General MOS modelling problems are presented and a set of workable solutions are developed. Experience with these techniques is shown along with examples of NMOS simulation applications. This paper discusses a technique with specific conventions for modelling MOS devices at the "logical transistor" gate level. The technique is not the optimal general solution, but was found to be satisfactory for retrofitting an existing 4-state logic simulator to include MOS capabilities. The technique is not meant to replace analog circuit simulation, but is aimed at increasing the accuracy of MOS logic (gate level) simulations. We begin with a general bus model and extend it to handle transistors, pullups and pulldowns, and dynamic MOS transfer gates. Extensions are shown for a bidirectional transfer gate model that can be connected in any topological configuration.

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8 V. D. Agrawal , A. K. Bose , P. Kozak , H. N. Nham , E. Pacas-Skewes, A mixed-mode simulator, Proceedings of the seventeenth design automation conference on Design automation, p.618-625, June 23-25, 1980, Minneapolis, Minnesota, United States

9 H. N. Nham , A. K. Bose, A multiple delay simulator for MOS LSI circuits, Proceedings of the 17th conference on Design automation, p.610-617, June 23-25, 1980, Minneapolis, Minnesota, United States

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12 P. Kozak , H. K. Gummel , B. R. Chawla, Operational features of an MOS timing simulator, Proceedings of the 12th design automation conference, p.95-101, January 1975

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14 Yacoub M. El-ziq, Logic design automation of MOS combinational networks with fan-in, fan-out constraints, Proceedings of the 15th conference on Design automation, p.240-249, June 19-21, 1978, Las Vegas, Nevada, United States

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Robert M. McDermott, Transmission gate modeling in an existing three-value simulator, Proceedings of the nineteenth design automation conference, p.678-681, January 1982

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Z. Barzilai , L. Huisman , G. Silberman , D. Tang , L. Woo, Simulating pass transistor circuits using logic simulation machines, Proceedings of the twentieth design automation conference on Design automation, p.157-163, June 27-29, 1983, Miami Beach, Florida, United States

Tsuyoshi Takahashi , Satoshi Kojima , Osamu Yamashiro , Kazuhiko Eguchi , Hideki Fukuda, An MOS digital network model on a modified thevenin equivalent for logic simulation, 21st Proceedings of the Design Automation Conference on Design automation, p.549-555, June 25-27, 1984, Albuquerque, New Mexico, United States

↑ INDEX TERMS

Primary Classification:
B. Hardware
↳ **B.7** INTEGRATED CIRCUITS
↳ **B.7.1** Types and Design Styles

Additional Classification:
B. Hardware
↳ **B.7** INTEGRATED CIRCUITS
↳ **B.7.2** Design Aids
↳ **Subjects:** Simulation

C. Computer Systems Organization
↳ **C.4** PERFORMANCE OF SYSTEMS
↳ **Subjects:** Modeling techniques

General Terms:
Design, Performance, Verification

Keywords:
Bus logic, Logic simulation, MOS models, Node models, Transfer gates

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#17 (((delay model<in>metadata) <and> (wire<in>metadata))<A...

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#19 (bus model<in>metadata)

#20 (((bus model<in>metadata))<AND>(verilog<in>metadata))

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1. **A new performance driven placement method with the Elmore delay mod VLSIs**
   Koide, T.; Ono, M.; Wakabayashi, S.; Nishimaru, Y.; Yoshida, N.;
   Design Automation Conference, 1995. Proceedings of the ASP-DAC '95/CHDL IFIP International Conference on Hardware Description Languages; IFIP Interr Conference on Very Large Scale Integration., Asian and South Pacific
   29 Aug.-1 Sept. 1995 Page(s):405 - 412
   Digital Object Identifier 10.1109/ASPDAC.1995.486252
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IEE JNL	IEE Journal or Magazine
IEEE CNF	IEEE Conference Proceeding
IEE CNF	IEE Conference Proceeding
IEEE STD	IEEE Standard

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1. **Intertwined development and formal verification of a 60× bus model**
Kaufmann, M.; Pixley, C.;
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12-15 Oct. 1997 Page(s):25 - 30
Digital Object Identifier 10.1109/ICCD.1997.628845
AbstractPlus | Full Text: PDF(668 KB) IEEE CNF

2. **Formal verification of a bus structure modeled in SystemC**
Habibi, A.; Tahar, S.; Halleb, L.;
Circuits and Systems, 2004. NEWCAS 2004. The 2nd Annual IEEE Northeast
20-23 June 2004 Page(s):61 - 64
Digital Object Identifier 10.1109/NEWCAS.2004.1359017
AbstractPlus | Full Text: PDF(389 KB) IEEE CNF

3. **A Verilog to C compiler**
Greaves, D.J.;
Rapid System Prototyping, 2000. RSP 2000. Proceedings. 11th International V
21-23 June 2000 Page(s):122 - 127
Digital Object Identifier 10.1109/IWRSP.2000.855208
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1. **A hybrid ASIC and FPGA architecture**
Zuchowski, P.S.; Reynolds, C.B.; Grupp, R.J.; Davis, S.G.; Cremen, B.; Troxel
Computer Aided Design, 2002. ICCAD 2002. IEEE/ACM International Confere
10-14 Nov. 2002 Page(s):187 - 194
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